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Solid State Research

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This technical report has been reviewed and is approved for publication.

FOR THE COMMANDER

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ABSTRACT

This report covers in detail the research work of the Solid State Division at Lincoln Laboratory for the period 1 August through 31 October 2001. The topics covered are Quantum Electronics, Electro-optical Materials and Devices, Submicrometer Technology, Biosensor and Molecular Technologies, Advanced Imaging Technology, Analog Device Technology, and Advanced Silicon Technology. Funding is provided by several DoD organizations—including the Air Force, Army, MDA, DARPA, Navy, NSA, and OSD—and also by the DOE, NASA, and NIST.

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A robust, miniature Ti:Sapphire laser system produces 14-μJ, 780-nm pulses of 1-ns duration at 10 kHz. The system is pumped by two fiber-coupled 808-nm laser diode arrays and occupies a volume of <0.5 liters.

2. ELECTRO-OPTICAL MATERIALS AND DEVICES

AlGaAsSb/GaSb quarter-wave distributed Bragg reflectors have been grown for the first time by organometallic vapor-phase epitaxy. The peak reflectance is 96% for a 10-period structure.

A high concentration of phosphorus vapor has been generated inside a plugged process tube by heating GaP or InP and by selectively condensing out the Group III species. This clean and controllable source eliminates the use of toxic gases and minimizes the production of hazardous wastes.

3. SUBMICROMETER TECHNOLOGY

A novel lift-off technique has been developed to pattern thick dielectric layers using a sacrificial layer of aluminum. This process has been used to fabricate the stator component for a micromotor.

4. BIOSENSOR AND MOLECULAR TECHNOLOGIES

Two simple, fast protocols, called Simple Nucleic Acid Prep (SNAP) and Affinity Magnet, have been developed for the collection and extraction of nucleic acids from environmental and clinical samples. Bacterial cells have been extracted in vegetative and spore form from a variety of solids, liquids, and solid surfaces, down to concentrations as low as 10 cells/mL or gram of target-containing material, and the SNAP protocol has been implemented into a simple cartridge format that has been successfully used for extraction of *Bacillus anthracis*.

5. ADVANCED IMAGING TECHNOLOGY

A scalable integrated circuit architecture has been developed, designed to support photon-counting intensity-imaging avalanche photodiode arrays. This architecture supports design of high-pixel-count imaging arrays.

6. ANALOG DEVICE TECHNOLOGY

A novel architecture has been developed for high-speed analog-to-digital conversion (ADC). A physical implementation of the delay-line ADC is currently being built and tested using off-the-shelf components.

7. ADVANCED SILICON TECHNOLOGY

Fully depleted silicon-on-insulator (FDSOI) technology is shown to be compatible with the construction of three-dimensional (3D) integrated circuits. Removal of the silicon substrate, an essential step in the 3D assembly technology, will not cause an increase in off-state current, provided the wafer bond technology is compatible with a 400°C sinter, and the substrate removal will also decrease the effect of ionizing radiation on transistor properties as well as improve rf performance.

REPORTS ON SOLID STATE RESEARCH
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Review of Technology for 157-nm Lithography	A. K. Bates M. Rothschild T. M. Bloomstein T. H. Fedynyshyn R. R. Kunz V. Liberman M. Switkes	*IBM J. Res. Dev.* **45**, 605 (2001)
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Microwave-Frequency Vortex Dynamics in YBCO Grain Boundaries	H. Xin D. E. Oates G. Dresselhaus* M. S. Dresselhaus*	*J. Supercond.* **14**, 637 (2001)

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On-Chip Membrane Maker	M. Hollis	BioFlips PI Meeting, Honolulu, Hawaii, 8-10 August 2001
Membrane Maker—Towards On-Chip Artificial Cells	L. Parameswaran J. Harper M. Hollis	BioFlips PI Meeting, Honolulu, Hawaii, 8-10 August 2001
Hydride Vapor Phase Epitaxial Growth of III-V Nitride Devices	R. J. Molnar	13th American Conference on Crystal Growth and Epitaxy, Burlington, Vermont, 12-16 August 2001
Use of In-Situ Spectral Reflectance for Rapid Analysis, Diagnostics, and Fundamental Studies of GaSb, GaInAsSb, and AlGaAsSb Epitaxial Layers	C. J. Vineis C. A. Wang K. F. Jensen*	13th American Conference on Crystal Growth and Epitaxy, Burlington, Vermont, 12-16 August 2001
High-Reflectivity AlGaAsSb/GaSb Mirrors Grown by Organometallic Vapor Phase Epitaxy	C. A. Wang D. R. Calawa	13th American Conference on Crystal Growth and Epitaxy, Burlington, Vermont, 12-16 August 2001

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Flux-Based Superconducting Qubits for Quantum Computation	K. K. Berggren T. P. Orlando* S. Lloyd* L. Levitov* M. Feldman* M. Bocko* M. Tinkham* J. Yepez*	European Applied Superconductivity Conference, Copenhagen, Denmark, 26-30 August 2001
Nonlinear Microwave Surface Impedance of YBCO Films: Latest Results and Present Understanding	D. Oates M. A. Hein* P. J. Hirst* R. G. Humphreys* G. Koren* E. Polturak*	European Applied Superconductivity Conference, Copenhagen, Denmark, 26-30 August 2001; Technical Seminar, Research Center, Karlsruhe, Germany, 31 August 2001; Technical Seminar, University of Wuppertal, Wuppertal, Germany, 3 September 2001; Technical Seminar, QinetiQ, Malvern, United Kingdom, 6 September 2001
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High-Brightness Tapered Laser Sources Emitting in the 1.3- to 2.0-μm Wavelength Range	J. N. Walpole* J. P. Donnelly H. K. Choi* Z. L. Liau L. J. Missaggia R. J. Bailey S. H. Groves G. W. Turner P. J. Taylor	Ultrafast Nonlinear Optics and Semiconductor Lasers Workshop, Cork, Ireland, 5-8 September 2001
Scaling Silicon to Its Limits: Will Optical Lithography Still Be Used?	D. C. Shaver	IEEE Lasers and Electro-Optics Society, Chapter Meeting, Lexington, Massachusetts, 13 September 2001
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CANARY B-Cell Sensor for Rapid Identification of Pathogens	M. Petrovick	BioMEMS and Biomedical Nanotechnology World 2001, Columbus, Ohio, 22-25 September 2001
Substrate Preparation and Low-Temperature Boron Doped Silicon Growth on Wafer-Scale Charge-Coupled Devices by Molecular-Beam Epitaxy	S. D. Calawa B. E. Burke P. M. Nitishin A. H. Loomis J. A. Gregory T. A. Lind	20th North American Conference on Molecular Beam Epitaxy, Providence, Rhode Island, 1-3 October 2001

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Characterization of Fully Depleted SOI Transistors after Removal of the Silicon Substrate	J. A. Burns K. Warner C-L. Chen P. M. Gouker	27th Annual IEEE International SOI Conference, Durango, Colorado, 2-4 October 2001
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Investigation of the Physical and Practical Limits of Dense-Only Phase Shift Lithography for Circuit Feature Definition	B. Tyrrell M. Fritze D. Yost D. Astolfi D. Chan* P. Rhyins*	21st Annual BACUS Symposium on Photomask Technology and Management, Monterey, California, 2-5 October 2001
GaInAsSb Materials for Thermophotovoltaic Devices	C. A. Wang C. J. Vineis R. H. Huang M. K. Connors H. K. Choi* L. R. Danielson* G. Nichols*	5th Conference on Thermophotovoltaic Generation of Electricity, Como, Italy, 8-10 October 2001

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HTS Technology for Analog Signal Processing	W. G. Lyons A. C. Anderson D. E. Oates	Lincoln Laboratory Technical Seminar Series, University of Rhode Island, Kingston, Rhode Island, 17 October 2001
Optical Sampling for Analog-to-Digital Conversions	P. W. Juodawlkis J. J. Hargreaves R. D. Younger R. C. Williamson G. E. Betts J. C. Twichell	Technical Seminar, National Security Agency, College Park, Maryland, 31 October 2001

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1. QUANTUM ELECTRONICS

1.1 MINIATURE, PULSED Ti:SAPPHIRE LASER SYSTEM

A miniature Ti:Sapphire laser system, producing 18.4-μJ, 780-nm pulses of 700-ps duration at 10-kHz repetition rate, was constructed and characterized. The system comprises a passively Q-switched microchip laser, an optical amplifier, a frequency-doubling crystal, and a miniature, gain-switched Ti:Sapphire laser. It is pumped with an average power of 17 W from two fiber-coupled laser diode arrays and occupies a volume of <0.5 liters. The optical layout and a photograph of the system are shown in Figures 1-1 and 1-2.

The passively Q-switched microchip laser comprises crystals of YAG, Nd^{3+}:YAG, Cr^{4+}:YAG, and YAG, diffusion bonded to each other in the order listed, with a 60% output coupler. Similar devices are reported elsewhere [1]–[3]. The laser is end pumped with the 808-nm output of a fiber-coupled high-power diode laser array. The pump array is operated in pulsed mode — the diodes are turned on by a clock signal and turned off when an output pulse is generated by the microchip laser — with a typical peak power of 17 W and pulse duration of 50 μs. The microchip laser has been operated at repetition rates from 0 to 20 kHz with a nearly constant pulse energy of 65 μJ. The output is single frequency and near diffraction limited, with stable 550-ps (full width at half-maximum) output pulses.

The output of the microchip laser is focused into a double-pass amplifier. The amplifier comprises crystals of YAG, Nd^{3+}:YAG and YAG, diffusion bonded to each other. It is end pumped with a second fiber-coupled high-power diode laser array, slaved to the diodes used to pump the laser. The output of the microchip laser is incident on the amplifier at a small angle. It is transmitted through the output facet and reflects off of the pump facet. At a repetition rate of 10 kHz, the beam exiting the amplifier has a pulse energy of 200 μJ and is ~1.2× diffraction limited.

KTP is used to frequency double the output of the amplifier, producing 90-μJ, 532-nm pulses. Before being focused into the KTP, the 1064-nm beam is filtered to remove residual pump light. The output of the KTP is filtered to remove residual 1064-nm light. Reflections from the filter are picked off and used to control the diode lasers.

The output from the KTP pumps a miniature gain-switched Ti:Sapphire laser [4]. The Ti:Sapphire laser has a cavity length of 9 mm. It comprises a 2.6-mm-long piece of highly doped Ti:Sapphire, a 60-μm-thick quartz etalon, a 200-μm-thick quartz etalon, a birefringent filter, and a concave 20% output coupler with a 2.5-cm radius of curvature. The Ti:Sapphire laser produces diffraction-limited 700-ps pulses with a pulse energy of 18.4 μJ at a pulse repetition rate of 10 kHz. When tuned to a center wavelength of 780 nm, the output bandwidth is 0.17 nm. The pulse-to-pulse amplitude stability is better than ±2%.

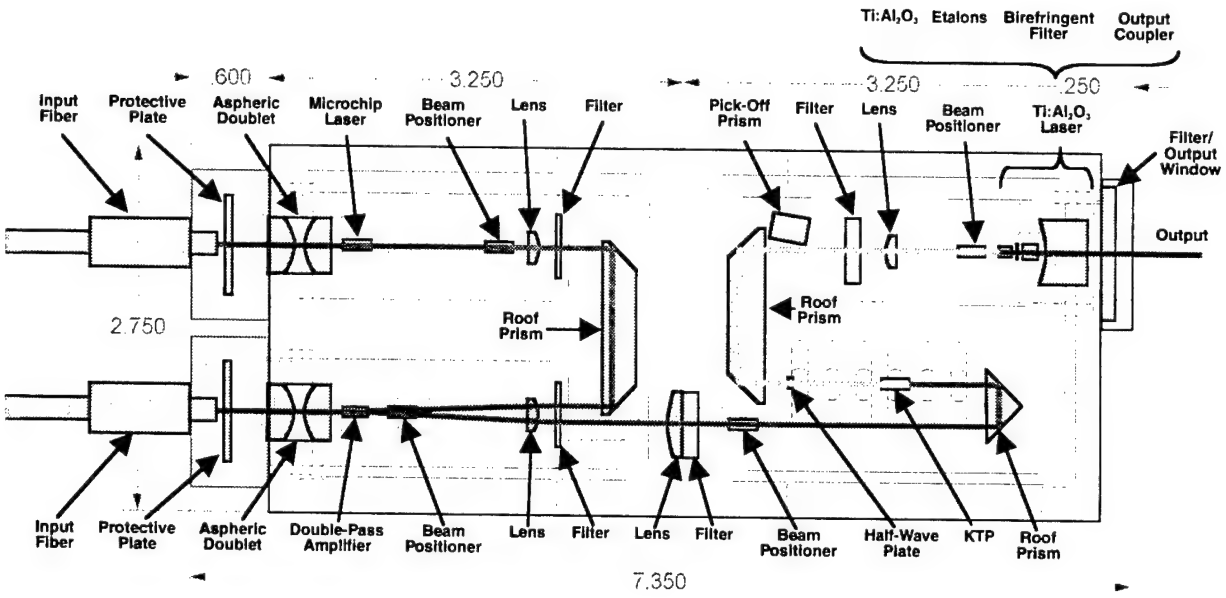

Figure 1-1. Optical layout of 18.4-μJ Ti:Sapphire laser system superimposed on mechanical drawing of support structure. Measurements shown are in inches.

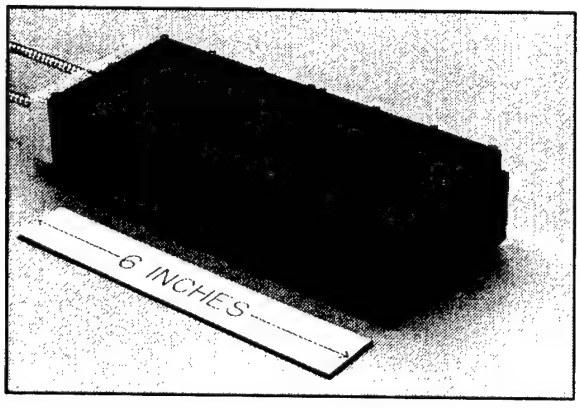

Figure 1-2. Photograph of 18.4-μJ Ti:Sapphire laser system.

By omitting the optical amplifier, a smaller version of the Ti:Sapphire laser system, occupying <0.2 liters, was realized. This system, shown in Figures 1-3 and 1-4, produces 5.5-μJ, 780-nm pulses, with pulse-to-pulse amplitude stability better than ±1%. The rest of the pulse characteristics are similar to the larger system.

J. J. Zayhowski
A. L. Wilson

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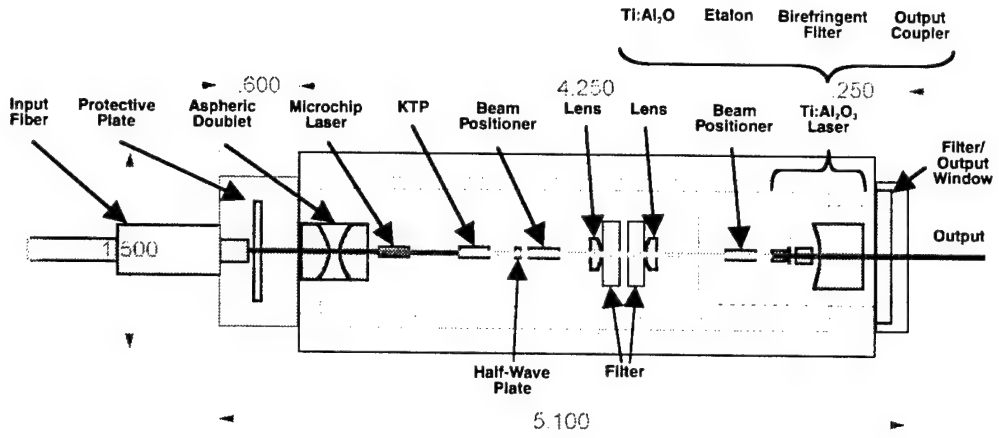

Figure 1-3. Optical layout of 5.5-μJ Ti:Sapphire laser system superimposed on mechanical drawing of support structure. Measurements shown are in inches.

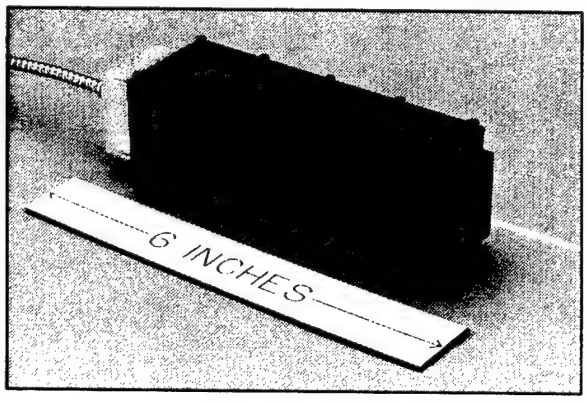

Figure 1-4. Photograph of 5.5-μJ Ti:Sapphire laser system.

2. ELECTRO-OPTICAL MATERIALS AND DEVICES

2.1 AlGaAsSb/GaSb DISTRIBUTED BRAGG REFLECTORS GROWN BY ORGANOMETALLIC VAPOR-PHASE EPITAXY

High-reflectivity mirrors have been shown to improve the performance of optoelectronic devices such as vertical-cavity surface-emitting lasers, resonant-cavity photodetectors, and photovoltaics. Al(Ga)As/GaAs quarter-wave distributed Bragg reflectors (DBRs) have been extensively used in GaAs-based devices [1], while AlGaAsSb/(Al)Ga(As)Sb DBRs have been incorporated in both InP- and GaSb-based devices [2],[3]. The AlSb-based materials for InP-based devices are attractive because these alloys have a larger index contrast than InP-based materials ($\Delta n \sim 0.6$ compared to 0.4), and consequently fewer periods are required for the same reflectivity. In addition, these alloys can be lattice matched to the InP substrate. However, the growth of AlSb-containing materials by organometallic vapor-phase epitaxy (OMVPE) is fundamentally more difficult [4],[5], and only molecular-beam epitaxy has been used to grow these AlGaAsSb/(Al)Ga(As)Sb DBRs. Since OMVPE is a leading technology for epitaxial growth of optoelectronic devices, it is important to develop OMVPE growth of AlGaAsSb/(Al)Ga(As)Sb DBRs. In this report, high-reflectivity AlGaAsSb/GaSb DBRs grown by OMVPE are reported for the first time.

GaSb and $Al_{0.81}Ga_{0.19}As_{0.06}Sb$ epitaxial layers were grown by OMVPE with all organometallic sources including tritertiarybutylaluminum, triethylgallium, tertiarybutylarsine, and trimethylantimony as described previously [4]. All layers were grown nominally lattice matched to vicinal (001) Te-doped GaSb substrates miscut 6° $\rightarrow$ (1-11)B. The growth temperature was 550°C. Accurate and reproducible layer thickness and composition must be accurately controlled for high-reflectivity DBR structures, and therefore, in-situ reflectance monitoring was used to calibrate growth rates and alloy composition [6].

AlGaAsSb/GaSb DBR structures were grown with 10 periods. The layer thickness was adjusted to vary the reflectance stop band from 1.6 to 2.4 μm. High-resolution x-ray diffraction was used to evaluate the structural quality, and the reflectance was measured with a Cary 5E spectrophotometer.

Figure 2-1 shows the in-situ spectral reflectance for growth of a typical AlGaAsSb/GaSb DBR structure at a monitoring wavelength of 633 nm. The intended layer thickness for this sample, which was designed to have a peak reflectivity at 2.2 μm, was 164.4 nm and 141 nm for AlGaAsSb and GaSb, respectively. The reflectance spectrum for growth of AlGaAsSb and GaSb layers is repeatable from one period to the next, which indicates that the growth is highly reproducible from layer to layer. Figure 2-2 shows the measured (upper) and simulated (lower) x-ray diffraction curves for the DBR structure. The simulation suggested layer thickness of 163.6 and 143.1 nm for AlGaAsSb and GaSb, respectively, and is in very good agreement with the intended layer structure. The high-order satellite peaks are indicative of excellent periodicity.

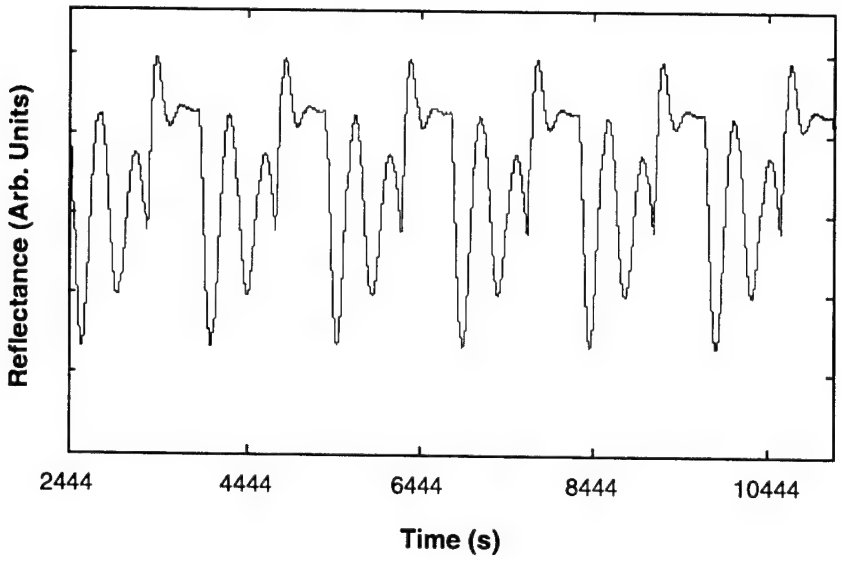

Figure 2-1. In-situ reflectance monitoring spectrum during growth of AlGaAsSb/GaSb distributed Bragg reflector (DBR) structure.

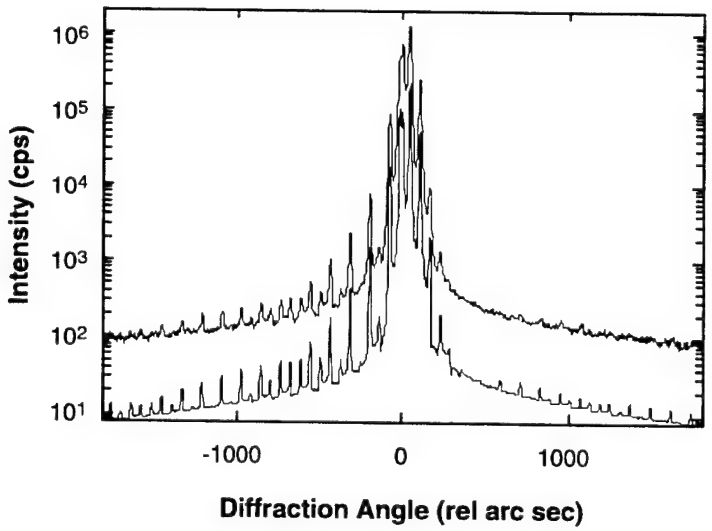

Figure 2-2. Measured (upper) and simulated (lower) high-resolution x-ray diffraction curves of 10-period AlGaAsSb/GaSb DBR structure.

The spectral reflectance measurement (solid line) and theoretical calculation (dashed line) are shown in Figure 2-3, and the agreement between the peak reflectance, width of the stop band, and side bands is excellent. A peak reflectance of 95.2% at 2.17 μm was measured. Optical constant data for AlGaAsSb used in the calculation were estimated by linear interpolation of the constituent binaries GaSb, AlSb, and AlAs [7].

Figure 2-4 summarizes the reflectance for four DBR structures, for which the reflectance stop band was adjusted by varying the thickness of AlGaAsSb and GaSb layers. The center of the stop band ranges from 1.59 to 2.47 μm, while the peak reflectance ranges from 93 to 96% for DBRs centered at 2.0–2.47 μm, and is 87.4% for the DBR centered at 1.59 μm. This lower value is due to absorption in the GaSb layer of the DBR. A low value of Al in this larger-index layer would increase the energy gap of that layer and thus decrease absorption, which will lead to increased reflectance.

In summary, AlGaAsSb/GaSb DBR structures have been grown successfully by OMVPE. Reflectance as high as 96% for a structure with only 10 periods was achieved. These results indicate that OMVPE growth of AlSb-based materials for DBR structures is extremely promising. Although this demonstration was for alloys lattice matched to GaSb substrates, it is expected that alloys lattice matched to InP can also be grown with success.

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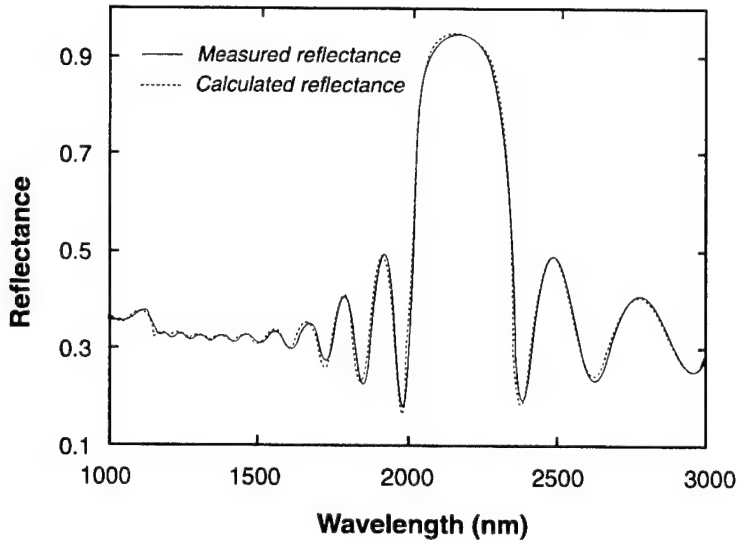

Figure 2-3. Measured (solid line) and calculated (dashed line) reflectivity spectra of 10-period AlGaAsSb/GaSb DBR.

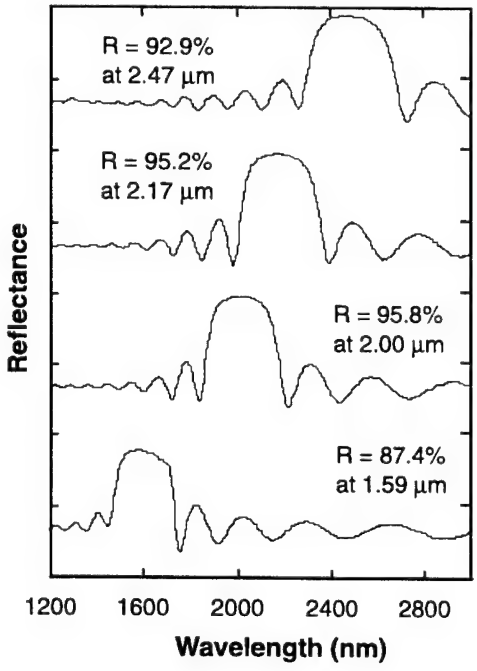

Figure 2-4. Spectral reflectivity of 10-period AlGaAsSb/GaSb DBR structures designed for various stop bands.

2.2 CLEAN CONTROLLABLE PHOSPHORUS-VAPOR SOURCE FOR SEMICONDUCTOR PROCESSING

Phosphorus overpressure is used in numerous semiconductor fabrication processes but is often difficult to implement because elemental phosphorus forms different isomers with a wide variation in vapor pressure, and the phosphorus deposits easily proliferate and result in contamination. Phosphine gas has been used for improved control but is highly toxic and hazardous [8]. Phosphide cover wafers and phosphorus-rich melt were used for wafer protection in earlier liquid-phase epitaxy work, but the process was rather crude and unoptimized. In this work, we developed a clean and highly controllable phosphorus vapor source without the use of toxic gases and with a minimum production of hazardous waste.

This phosphorus source has been developed primarily for GaP microlens fabrication by mass transport [8] at around 1100°C, in which high phosphorus vapor pressure is needed for complete wafer protection and optimum process results. As illustrated in Figure 2-5, phosphorus vapor is generated by placing GaP or InP at elevated temperatures in the furnace system. The use of InP has the advantage of lower source temperatures. To maintain a uniform high phosphorus vapor concentration and to minimize the source consumption, both the source and the main wafer are placed in a quartz process tube enclosed by a quartz plug.

In each experimental run, an initial baking period was used to drive out the room air, moisture, and organic adsorbates from inside the process tube. The outdiffusion can be accelerated by maintaining the plug region at a high temperature for increased gas diffusivity. Alternatively, a pumping action can be utilized by repeatedly heating and cooling the process tube. However, this procedure requires a longer furnace tube to allow sufficient furnace movement and was not extensively used in the present work. Nevertheless, additional pumping action inherent to the phosphorus outdiffusion could have helped in achieving a clean system.

The phosphorus vapor pressure inside the process tube is, in principle, determined by the source temperature. The equilibrium vapor pressure has been documented in published phase diagrams [9]. Experimentally, the actual vapor pressure is set by the steady state in which the vapor outdiffusion (or outflowing) rate equals the source evaporation rate. The latter can be estimated from the observed source consumption rate and was ~5 g of InP (1100°C) in 24 h. The vapor outdiffusion rate can be estimated from a room-temperature test measurement using a highly volatile liquid, e.g., methanol, of a known vapor pressure. In the case of a looser quartz plug (i.e., higher vapor outdiffusion rate), the phosphorus partial pressure is approximately given by the ratio of the source evaporation rate to the total vapor outdiffusion rate. In the other extreme case of a tight plug, the phosphorus vapor pressure can build up to surpass the Ar ambient pressure, since the equilibrium phosphorus vapor pressures at the temperatures used well exceed several atmospheres [9]. However, only a modest pressure gradient is likely needed to produce a flow rate equal to the observed source evaporation rate. The phosphorus vapor pressure inside the process tube is expected to be only slightly higher than the Ar ambient pressure which could be controlled between 1 and 3 atmospheres in the present work. While these estimates provide useful insights, the optimum parameters were determined experimentally for the best process results.

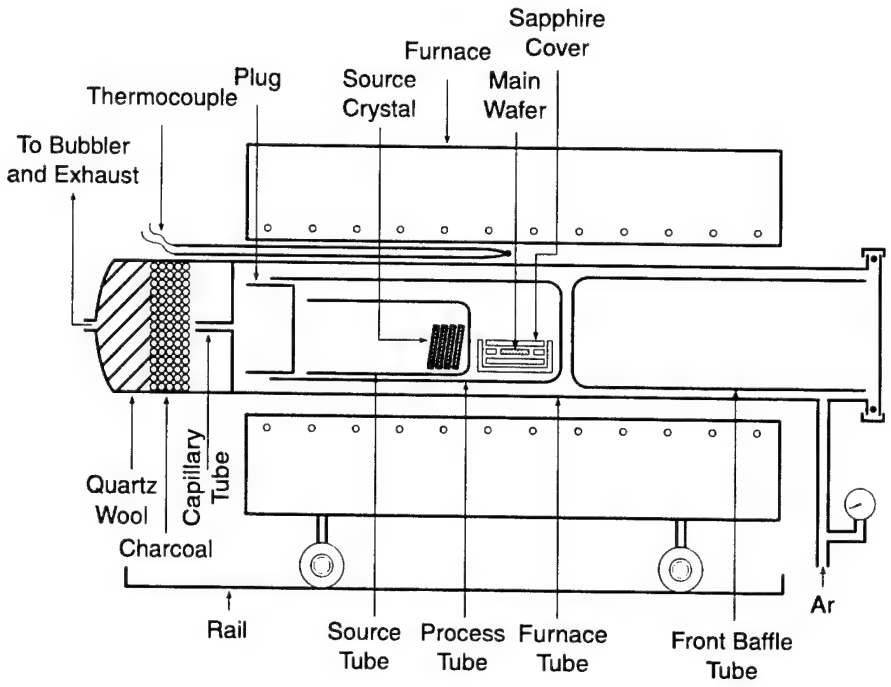

Figure 2-5. Illustration of the mass-transport furnace system with a clean controllable phosphorus-vapor source. The vapor is generated by source crystals of GaP or InP, but is passed through a cooler region near the mouth of the source tube in order to selectively condense out the Group III component. It should be noted that this drawing is highly schematic and not to scale.

While the bulk of the Group III component in the source gradually became a melt, there is a finite vapor pressure which can severely interfere with the mass-transport process. This was effectively prevented by placing the source in a test-tube-shaped quartz container, as illustrated in Figure 2-5. The vapor originating from the source is thus required to pass through a cooler zone of 400–500°C where the Group III species are selectively condensed out.

The outdiffusion of phosphorus from the process tube gradually led to an accumulation in the rear part of the furnace tube. When the system was opened for loading and unloading without a load-lock, oxygen and moisture were absorbed by the deposited phosphorus and could subsequently become a source of contamination. Also, the accumulated phosphorus can continuously migrate downstream to the entire exhaust system. These contaminations were effectively eliminated by the implementation of a capillary tube to prevent backdiffusion and a subsequent charcoal filter section with a quartz wool plug to contain the accumulated phosphorus. (It was necessary to heat the capillary tube to a moderate temperature during each run to prevent clogging.)

The present clean phosphorus-vapor source has been used for numerous mass-transport runs, ranging from 10 to >100 h, and has achieved excellent results. This demonstrates the effectiveness of the

present scheme, since mass transport, as a near-equilibrium surface process, requires high phosphorus-vapor concentration and is highly sensitive to trace contaminations. Possible further improvements include a better controlled plug, probably a tight one equipped with a capillary tube as a controlled leak.

The present scheme can be used for other types of phosphide processing and crystal growth. It can also be readily adapted for providing other vapors, such as arsenic. The elimination of toxic gases and minimization of hazardous wastes in the laboratory make it highly desirable for a number of semiconductor fabrication processes.

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3. SUBMICROMETER TECHNOLOGY

3.1 A NOVEL PROCESS FOR PATTERNING THICK DIELECTRIC LAYERS

Integrated circuit (IC) fabrication techniques, such as lithography, film deposition, and etching, have been applied to the production of complex, low-cost, miniature components for micro electro mechanical systems (MEMS). A major challenge unique to MEMS fabrication is the need to pattern thick dielectric layers. An example of this requirement is the electrostatic induction micromotor [1] being jointly developed at MIT Lincoln Laboratory and MIT Campus. The stator component for this micromotor must be fabricated on a thick insulating film to maximize the electrical performance of the motor. Mechanical and thermal considerations dictate that the insulating film be implemented as thick dielectric islands buried in the silicon substrate. This report describes a novel approach to fabricating this device which is applicable to numerous other MEMS components.

For traditional semiconductor fabrication, two approaches can be used to form features in materials: a subtractive process where either a wet chemical etch or plasma etch can be used to remove bulk material, or an additive approach in which layers are built up by selective deposition. The choice of a process depends upon considerations such as relative etch rates of the material being patterned with respect to the masking material, rates of deposition and etch, selectivity of the process, and desired profile of the finished feature.

Conventional subtractive patterning of thin films employs a masking layer, which is patterned lithographically. The mask pattern is then transferred into the desired film. The constraints on this approach are primarily the rate of loss of the masking material with respect to the layer being patterned. For example if the masking material has the same etch rate as the film being patterned, then only a thickness equivalent to the starting mask could be patterned into the underlying layer.

If an additive approach is used, a sacrificial layer is patterned with the inverse of the desired pattern, that is, the sacrificial layer is opened in the areas where a final film is desired. With the subsequent removal of the sacrificial layer, the film that had been deposited in the unwanted areas is also removed, leaving the desired pattern. Typically a photoimaged polymer resist is used as the sacrificial layer.

We have currently implemented a combination of both of the above techniques to pattern, at dimensions previously unachieved, thick buried silicon dioxide islands upon which high-power electrostatic induction motors have been fabricated. In this novel approach, an aluminum metallization is used as the sacrificial layer.

For the efficient performance of an electrostatic induction motor, the area upon which the stator electrodes are fabricated must have adequate electrical properties to hold off high voltages to prevent current leakage into the carrier silicon substrate. The material chosen upon which to build the stator is silicon dioxide owing to its high resistance, thermal stability, and compatibility with additional

semiconductor processes. Conventional subtractive patterning techniques have proven to be inadequate to pattern the required 20-μm-thick dielectric layer.

Figure 3-1 shows an idealized cross section of the stator, which would be one of five silicon wafers that are bonded together to form the entire micromotor. Platinum electrodes necessary for power generation are indicated on a 20-μm-thick silicon oxide film.

Our initial approach for patterning the 20-μm-thick oxide in the silicon pit is illustrated in Figure 3-2(a). First a 20-μm-deep pit was etched into our substrate wafer using a conventional photoresist mask followed by pattern transfer using a deep Si reactive ion etcher. The entire wafer is then covered with 1 μm of sputtered aluminum. The original photomask is re-imaged on the aluminum, and the exposed aluminum is removed in a wet etch. The result is a sacrificial aluminum layer over the entire wafer except in the 20-μm-deep pits. The wafer then receives a blanket deposition of 20 μm of plasma-enhanced chemical vapor deposition (PECVD) tetraethoxysilane (TEOS). Following the deposition, the perimeter of the wafer is lightly scribed to break through the oxide and expose the underlying aluminum. The wafer is then placed in a warm HCl bath, which selectively consumes the aluminum and simultaneously lifts off the 20 μm of TEOS on the entire wafer except for the silicon pit area, where the oxide tightly bonds to the silicon substrate. The wafer then receives a light chemical mechanical polish to remove oxide artifacts from around the pit edge, and the rest of the induction motor fabrication proceeds.

Detailed profilometry indicated that while this process flow was capable of satisfactory device profiles, artifacts occurred in which the oxide broke away at the junction of the field and the pit, and voids would occasionally develop around portions of the 20-μm pit. A typical artifact is shown in Figure 3-3. These artifacts created undesirable topography on the top surface of the oxide, which affected the

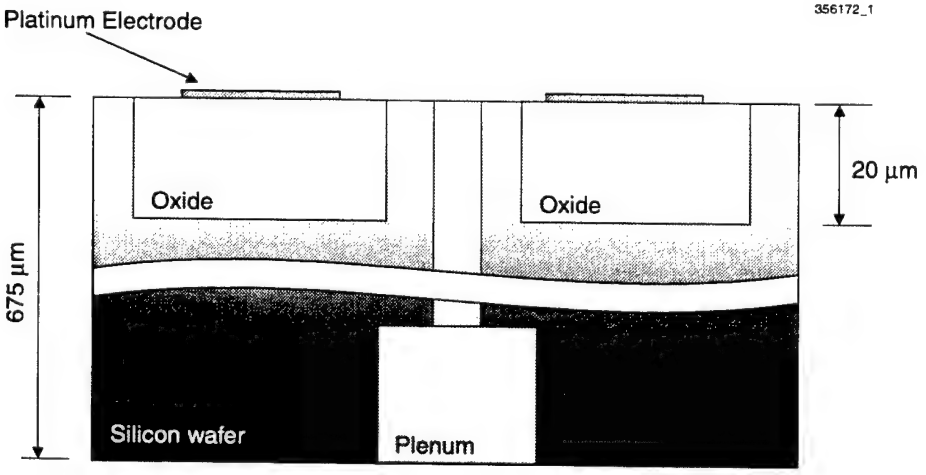

Figure 3-1. Idealized cross section of micromotor stator with platinum electrodes. This component is fabricated on a standard silicon wafer. The platinum electrodes are patterned on thick silicon dioxide islands embedded in the top surface of the wafer. The plenum etched through the wafer provides gas flow for the air bearing.

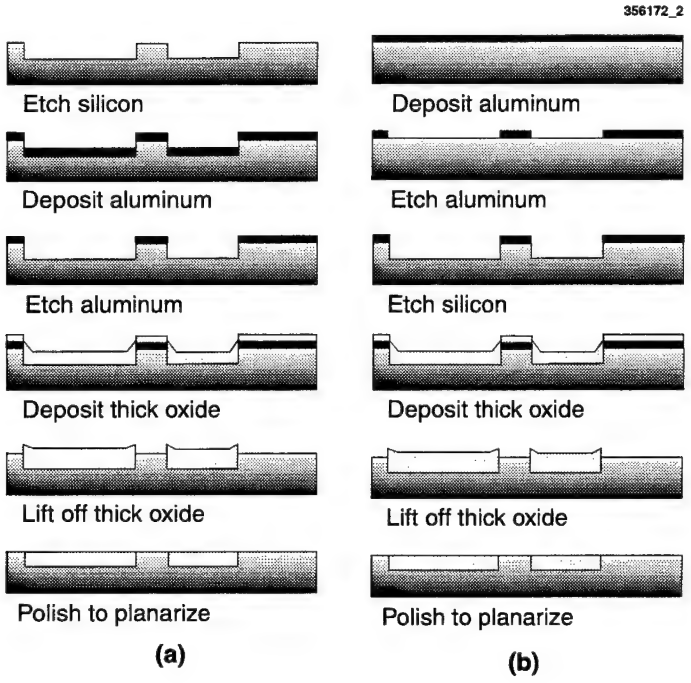

Figure 3-2. Alternative stator fabrication sequences. (a) Original process in which the silicon pits are etched first and then the sacrificial aluminum layer is deposited and patterned. Then the thick oxide is deposited and the aluminum layer is removed using a chemical etch that lifts off the unwanted oxide at the wafer surface. The wafer is then polished to planarize the surface. (b) Improved fabrication process in which the sacrificial aluminum layer is deposited on the unpatterned silicon surface. The aluminum is then patterned and the aluminum is used as a mask to etch the silicon. In the remaining steps the thick oxide is deposited, lifted off, and polished as in the original process flow.

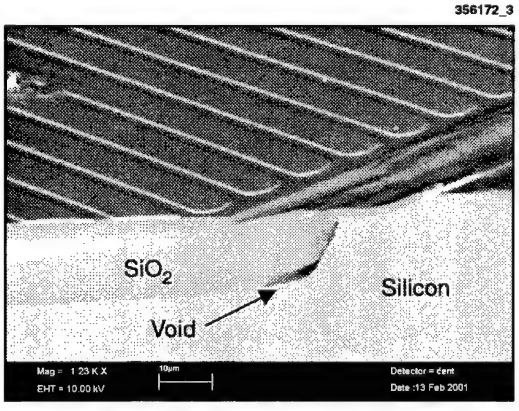

Figure 3-3. Scanning electron micrograph (SEM) illustrating the platinum electrode array patterned on the thick SiO_2 island embedded in the silicon substrate. Notice the undesirable void at the silicon-SiO_2 interface.

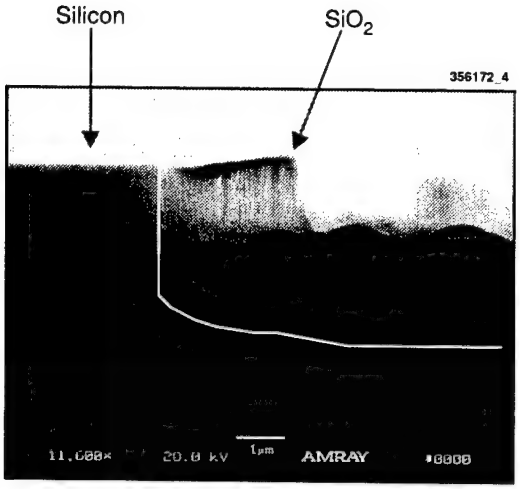

Figure 3-4. SEM cross section of silicon pit with oxide fill after lift-off. This sample was fabricated using the improved process illustrated in Figure 3-2(b). The interface between the silicon and the oxide is not distinct in this picture and has been marked with a white line. Notice that there are no voids in the oxide at the interface. In this test run the oxide was not sufficiently thick to fill the pit and a step is visible in the surface.

patterning of the platinum electrodes. The source of the voids is felt to be the difficulty in applying the photoresist over a 20-μm step when patterning the sacrificial aluminum. Incomplete removal of aluminum along the pit sidewall would leave a sacrificial film behind and possibly create a void during the HCl etch. The solution to this problem was found in reordering the process steps and eliminating a photoresist step, as seen in Figure 3-2(b). Now, instead of etching the deep pit into the silicon and then attempting to reproduce the photoresist step over steep topography, the aluminum is first patterned, and then the 20-μm pit is etched using the patterned aluminum layer as an etch mask. In this processing sequence the sacrificial aluminum is self-aligned with the silicon sidewall. There is no opportunity for the aluminum to remain on the sidewall and create voids during the HCl etch. At the top of the pit there is also much better dimensional control of the transition of the oxide to the bare silicon wafer after lift-off. Controlling the oxide surface, pit dimensions, and the oxide-silicon transition are crucial to obtaining good yield when patterning the platinum electrodes. Figure 3-4 illustrates the silicon-oxide interface patterned using this improved process flow.

The original aluminum lift-off technique has produced working devices demonstrating an order of magnitude more power than previous devices, with a power density of 16 kW/m^3 [2]. The improved processing approach will be used for future device fabrication.

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4. BIOSENSOR AND MOLECULAR TECHNOLOGIES

4.1 TECHNIQUES FOR THE EXTRACTION AND IDENTIFICATION OF DNA IN ENVIRONMENTAL SAMPLES

The ability to rapidly and accurately detect trace levels of bacterial organisms from environmental and clinical samples is of vital importance for biodefense, forensics, and clinical diagnostics. In light of recent events involving bioagent releases, this capability has taken on even more importance. Currently, the most accurate method of identifying a target organism is via the polymerase chain reaction (PCR). PCR uses a thermostable enzyme called DNA polymerase to amplify small numbers of nucleic acid molecules into much larger quantifiable amounts. The copies can be "counted" by tagging each molecule with a fluorescent probe, and measuring fluorescence intensity as the reaction progresses. Identification is achieved by selectively amplifying and counting only those genetic sequences that match the desired target organism(s).

Cleanup of the sample to be amplified is often the critical step, as PCR is sensitive to changes in solution conditions, including pH, temperature, and molecules that inhibit the action of the polymerase. These inhibitory molecules include hemoglobin in blood, magnesium and other cations in soils, and dyes in cloth. Thus, the ability to collect trace levels of bacterial cells and DNA from "dirty" samples and extract the contained nucleic acids, while eliminating any inhibitory molecules, is of prime importance.

We have developed two simple and fast sample preparation protocols, Simple Nucleic Acid Prep (SNAP) and Affinity Magnet, described in Figures 4-1 through 4-3. Using these protocols, we have been

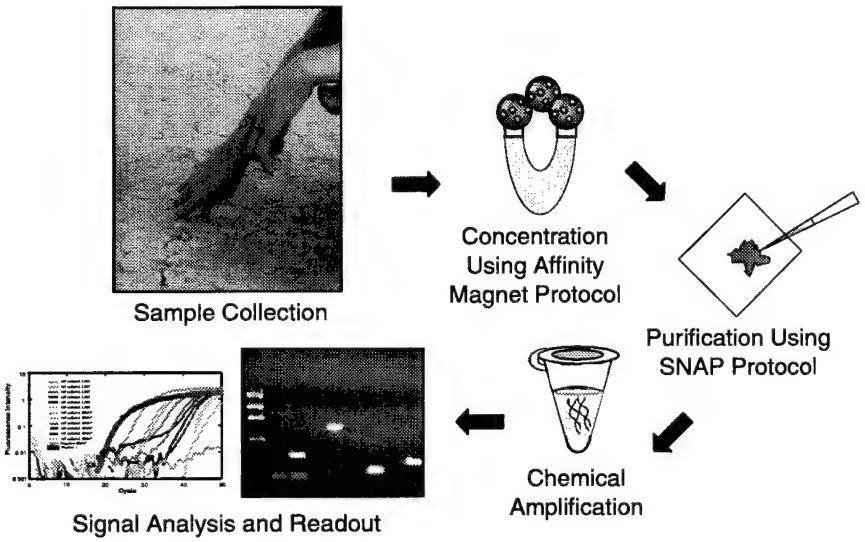

Figure 4-1. Overview of sample collection and processing.

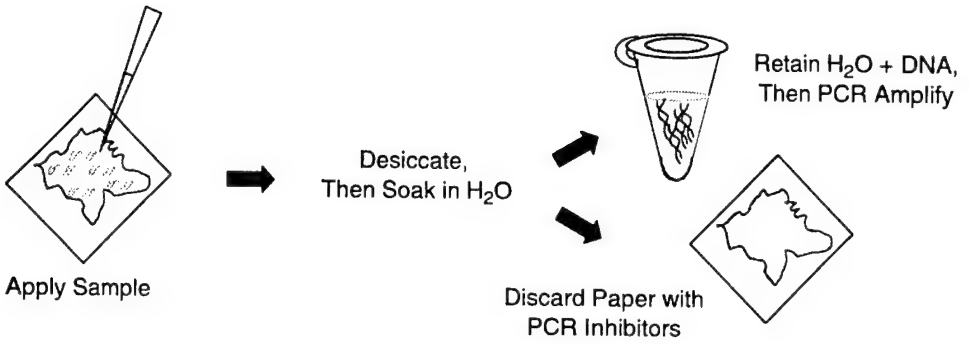

Figure 4-2. SNAP protocol for purification of nucleic acids.

able to successfully demonstrate extraction of bacterial cells (including *Bacillus anthracis* Stern strain, *Bacillus thuringiensis,* and *Yersinia pestis* KIM5 strain) in vegetative and spore form, from a variety of materials including soils, cloth, indoor and outdoor solid surfaces and foods, down to concentrations as low as 10 cells/mL or gram of target-containing material.

The central element of the SNAP protocol, as shown in Figure 4-2, is a chemically treated paper (IsoCode, manufactured by Schleicher & Schuell). This paper is able to lyse cells, bind inhibitors to PCR, and release nucleic acids. The SNAP protocol is simple and fast, as it requires only water as a reagent and can be done in less than 30 min. It can also be implemented in field-portable format when the paper is incorporated into cartridges, as will be discussed later. Additionally, the lysis capability of the paper ensures that the target cells are inactivated and made safe for transport. The nucleic acids can also be archived on the paper, as has been demonstrated by us, as well as by Schleicher & Schuell with blood samples archived for years.

The Affinity Magnet protocol uses magnetic beads, illustrated in Figure 4-3, with surface coatings having affinities for vegetative cells, spores, and DNA. The protocol exploits the natural hydrophobic or hydrophilic surface properties of the target cells and DNA to bind to and remove them. Other more specific binding affinities can also be used by tailoring the magnetic bead coatings to incorporate such molecules as peptides having affinities to surface coat proteins, antibodies, or other chemical groups. The Affinity Magnet protocol is illustrated in Figure 4-4.

We have exercised these protocols on a wide variety of sample materials (matrices), including soils (10^1–10^3 cells/g), cloth, milk (10^3 cells/mL), meat homogenate (10^3 cells/g), blood (10^2 cells/mL), and saliva; detection limits to date are given in parentheses. We have been able to detect *B. anthracis* Stern strain and *B. thuringiensis*, in both vegetative and spore form, and *Y. pestis*. We have also been able to detect target from samples that have been decontaminated via bleaching and/or autoclaving. Initially, results were obtained via separation of the PCR-amplified DNA using gel electrophoresis, to determine the presence of DNA of the appropriate size to match the desired target. Subsequently, we purchased an ABI

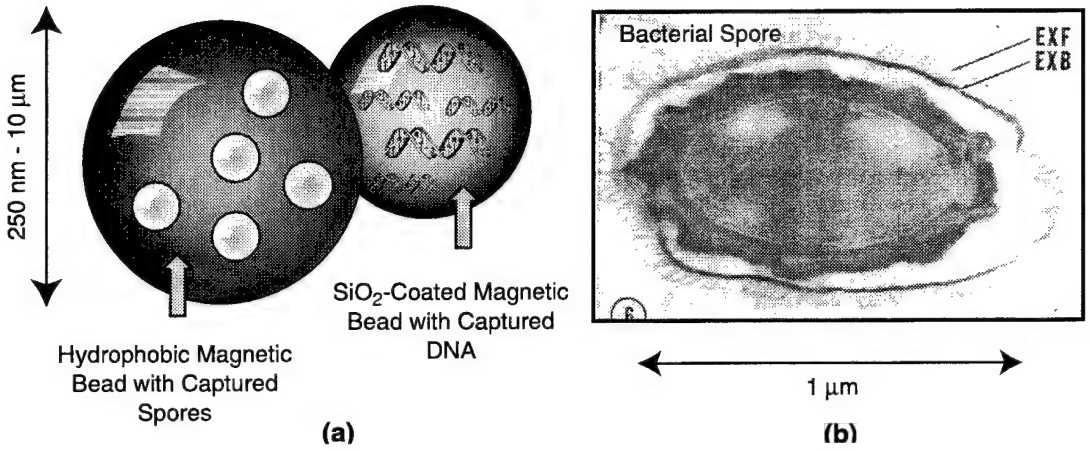

Figure 4-3. (a) Illustration of magnetic beads used in Affinity Magnet protocol and (b) electron micrograph of bacterial spore, showing hairy exosporium.

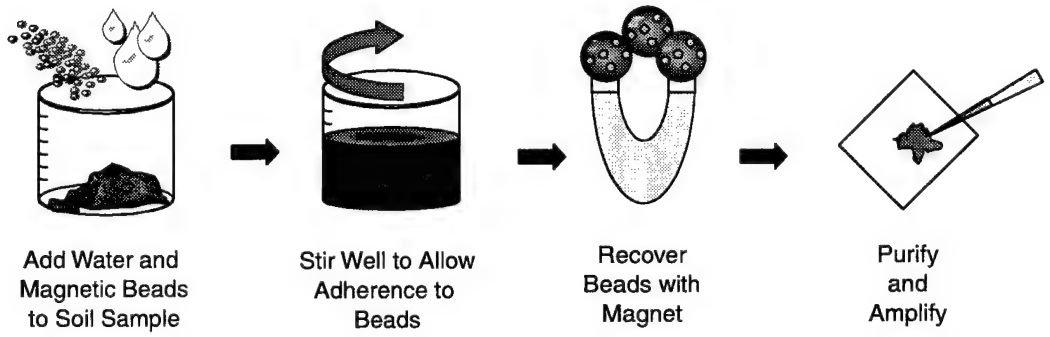

Figure 4-4. Affinity Magnet protocol for concentration of target.

Prism 7700 Sequence Detection System (manufactured by Applied Biosystems), which is capable of real-time detection of PCR products using the TaqMan fluorogenic 5′ nuclease assay. The ABI 7700 provides a 10^3 improvement in detection limits over the gel-based method.

We have done preliminary investigations to implement the Affinity Magnet protocol in larger-scale format, using chaotic mixing techniques to enhance interaction of the magnetic beads with the target matrices. This has enabled us to handle gram quantities of matrix, rather than the milligram quantities used for the majority of our experiments. We are considering the design of more sophisticated apparatuses, such as those incorporating vanes for increased surface area, in order to improve mixing efficiency.

We have also investigated the use of electric fields to enhance removal of DNA from IsoCode paper, exploiting the fact that the negatively charged DNA will migrate to a positive electrode in the presence of an electric field of sufficient strength. Experiments are ongoing in this area.

As a means of further simplifying the SNAP protocol, we also have looked into reducing the time and temperature required to remove (elute) the DNA from the IsoCode. We have found that it is possible with some matrices to reduce elution times down to a few minutes or less, and eliminate the heat requirement altogether. This has significant impact on fieldability of the protocol, as it greatly reduces power and time requirements.

While the SNAP and Affinity Magnet protocols are simple and fast, a need exists to implement them in an easy-to-use, field-portable format. Towards that end, we have considered various ways to implement the IsoCode paper and required reagents, as well as storage, archiving, and sample processing functions, into a compact, field-portable cartridge. We currently have in place a subcontract with Environmental Technologies Group Inc. (ETG) and Edge Medica to develop such a device.

Owing to the recent urgent need for improved sampling techniques, we quickly developed an initial simple version of the cartridge, implementing only the SNAP protocol. The device is based on a commercially available syringeless filter called the Mini-Uniprep, manufactured by Whatman, which we have modified by replacing the filter membrane with a version of IsoCode that is thicker and contains a smaller amount of the lysis chemical. Referred to as the LINK (Lincoln Interim Nucleic-acid Kit) cartridge, this device is shown in Figure 4-5, and its use illustrated in Figure 4-6.

This format greatly simplifies sampling, and enables the easy collection and safe transport of liquid samples as well as solid surface wipes. We have used the LINK cartridge to extract vegetative *B. anthracis* from air-to-liquid samples taken from field collection units, with detection demonstrated down to levels of 1 cell/mL, as shown in Figure 4-7. Other successfully detected samples include wipes from humans and various laboratory and office surfaces. We have also recently demonstrated successful detection of both

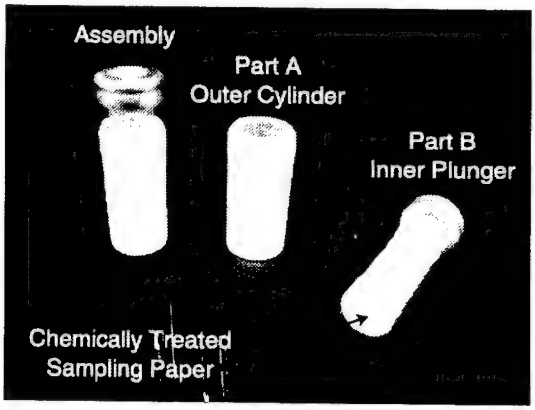

Figure 4-5. Lincoln Interim Nucleic-acid Kit (LINK) cartridge.

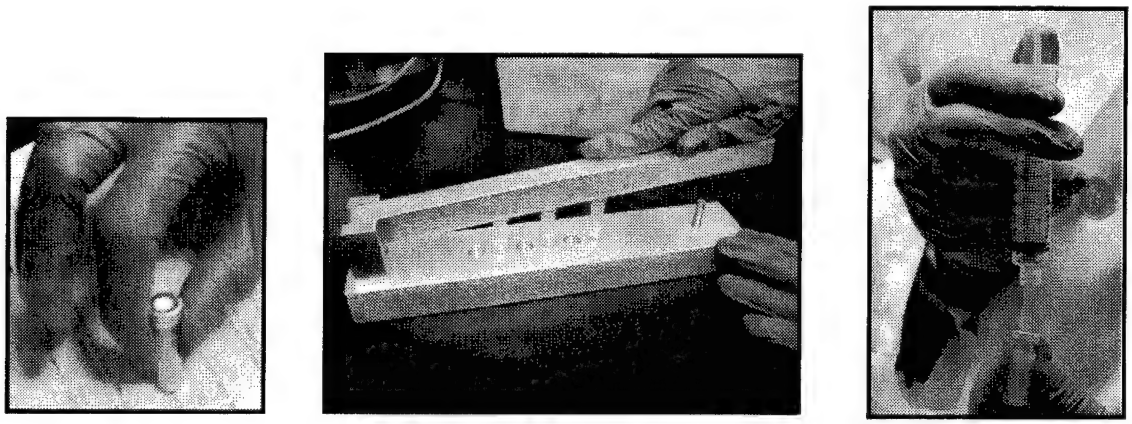

Figure 4-6. Steps in use of LINK cartridge shown in Figure 4-5: (a) Wipe surface, (b) force plunger into outer cylinder to process in one step, and (c) remove DNA and analyze. The total time is approximately 5 min. Note that step (b) may be done manually or with a clamp. Samples may also be deposited in liquid form onto the end of the plunger.

vegetative and spore forms of *B. anthracis* in tests at the U.S. Army Medical Research Institute of Infectious Diseases. Detection was comparable to that obtained with their conventional protocol (Qiagen kit), but sample preparation was completed in a fraction of the time.

We are working with a group of biomedical and environmental sampling device companies (ETG, Edge Medica, and Cepheid) to further the LINK concept, as well as develop more advanced versions that incorporate magnetic beads for target concentration from semi-solid and viscous slurry samples. With some modifications, it may also be possible to use the LINK cartridge to collect aerosol samples via direct air impaction onto the IsoCode surface of the cartridge. Such an approach, combined with the Biological Agent Warning Sensor (BAWS) as a trigger, and a handheld PCR unit, could enable the rapid collection, analysis, and identification of bioagents in many field scenarios.

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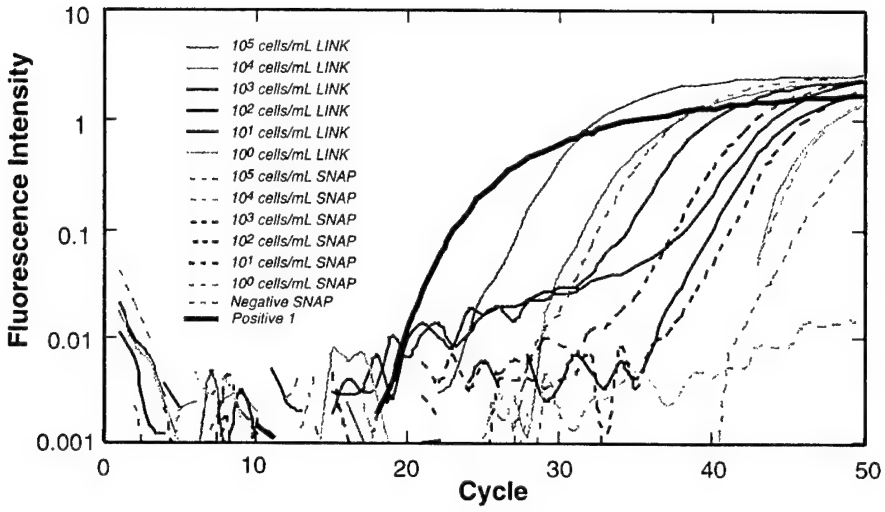

Figure 4-7. Demonstration of detection of B. anthracis seeded into air-to-liquid field samples. Detection down to 1 cell/mL was obtained, with the LINK cartridge showing reduced detection cycle thresholds, as compared to the normal SNAP protocol, at all seeding levels. Detection cycle threshold is defined as the cycle at which the fluorescence intensity (Rn) exceeds 0.1; a lower cycle threshold indicated that a higher initial number of copies of DNA was present in the original sample subjected to amplification, and/or that less inhibitors were present in the sample.

5. ADVANCED IMAGING TECHNOLOGY

5.1 SCALABLE CMOS READOUT CIRCUIT ARCHITECTURE FOR PHOTON-COUNTING APPLICATIONS USING GEIGER-MODE AVALANCHE PHOTODIODES

Integration of Geiger-mode avalanche photodiodes (APDs) with high-speed digital readout circuits has opened up the possibility of building photon-counting focal-plane-array intensity imagers [1],[2]. These imagers are distinguished from other solid state sensors by the absence of readout noise, since data are directly collected in digital form and therefore no equivalent analog-to-digital conversion of an electric signal is needed. A single photon detected by an APD is sufficient to generate a digital signal level that will trigger a CMOS circuit, thereby allowing direct photon-to-digital conversion to take place in the pixel. Here, we describe a scalable integrated circuit architecture that we have developed, which is designed to support photon-counting intensity-imaging APD arrays. This architecture supports design of high-pixel-count imaging arrays.

The design objectives for this imager circuit architecture were: (1) compact pixel footprint, (2) large dynamic range, (3) photon count rates as high as 10^7 photons per second per pixel, (4) low power dissipation per pixel of 0.1 μW, and (5) flexibility and adaptability to many sizes and variations. This circuit architecture was developed to meet these objectives.

The primary requirement was to design a pixel circuit that is capable of being implemented in a reasonably small footprint using commercially available CMOS. Figure 5-1 shows a 10-transistor pixel circuit design that digitally stores a single bit of information that indicates whether or not a photon was detected by the APD between interrogations. This circuit was designed in a 0.35-μm CMOS process, resulting in a pixel with a length of 15 μm on a side, considered small enough to meet the first design objective.

The pixel circuit performs the functions of arming the APD, actively quenching the APD if it is triggered within a set gate time, storing the bit value, and disarming the APD after the set gate time. Limiting the pixel storage to just one bit allows necessary control of the dead time of the APD element (the time the APD must "rest" after having avalanched). However, single-bit pixel storage does require an architecture able to rapidly revisit the pixel (~10^7 Hz, comparable to the APD dead time) to determine its state. With each revisit cycle, the on-chip accumulator corresponding to that pixel is updated. The final accumulator result is the number of times the pixel has avalanched between off-chip readout events. The pixel circuit operates by dynamically storing the data bit on the gate of transistor M9, which is read out from the pixel through the bitline as an inverted value when the decoder line addressing that pixel row switches high. A high value stored on the gate of M9 indicates that the APD fired and will turn on that transistor, thereby discharging the bitline capacitance through the series combination of M9 and M10 when that pixel row is accessed by a read operation. Figure 5-2 shows a block diagram of the readout circuit architecture that supports this pixel circuit.

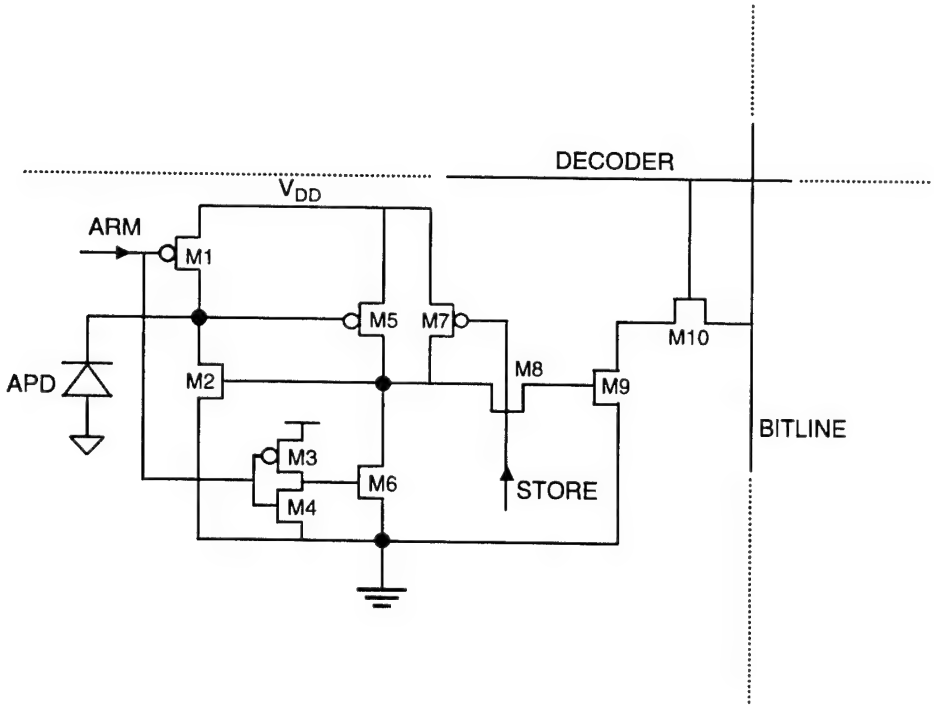

Figure 5-1. 10-Transistor active quenching pixel.

The pixels are arrayed in a matrix of n rows and m columns and are addressed using a row decoder with n outputs. Photon-counting accumulators are also arrayed in a matrix of n rows and m columns. The photon-counting accumulators are shown being addressed using a separate row decoder with n outputs, although a single decoder could be used to address both the pixel and accumulator arrays. A binary counter drives the two decoders simultaneously. A bitline-sensing circuit placed at the bottom of each column of pixels quickly converts the precharged capacitance of the bitline into a digital 0 or 1 during read operations. During normal imager operation, either an on-or-off chip programmable state machine would supply the control and clocking signals that are shown in Figure 5-3.

The APDs in the pixel array are gated on synchronously when the global ARM signal pulses low. At this point, each APD can be discharged by the avalanche multiplication of an electron-hole pair generated either by an absorbed photon or thermally. The store signal, distributed synchronously to all the pixels, transitions low at the end of the gate time interval storing a data bit in the pixel and subsequently disarming the APD, marking the start of the APD dead time. The pixel data are then read out to an array of on-chip accumulators, located outside the imaging area. Each accumulator counts the number of photons that have been detected by its corresponding APD between off-chip read cycles. For large arrays, the readout cycle just described could be speeded up by partitioning the rows of the pixels and accumulator arrays into

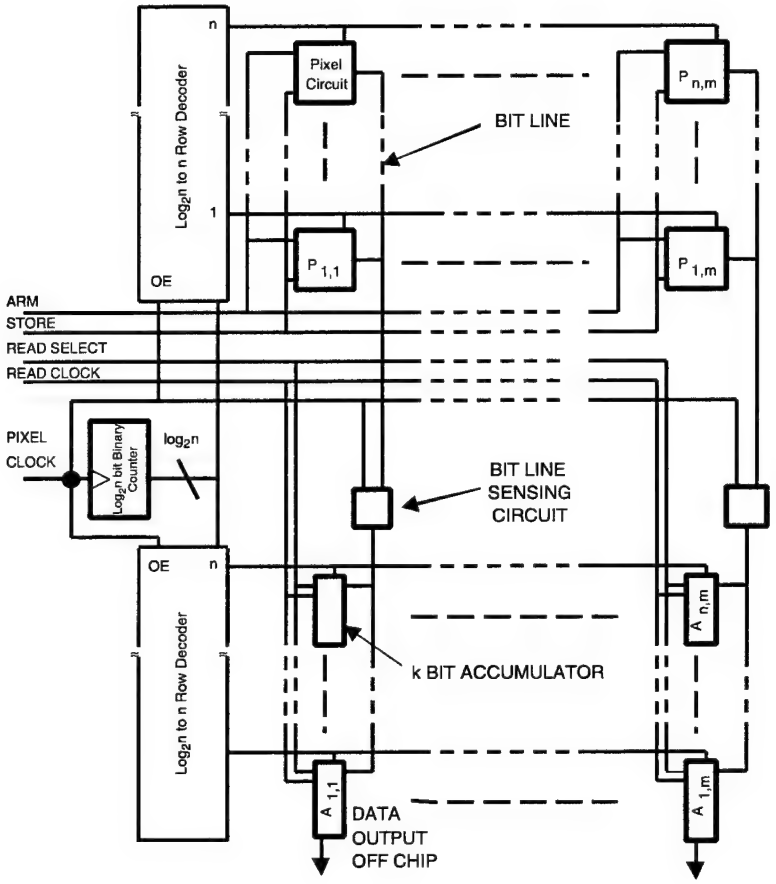

Figure 5-2. Imager readout circuit block diagram: n (row) × m (column) APD pixel and accumulator arrays.

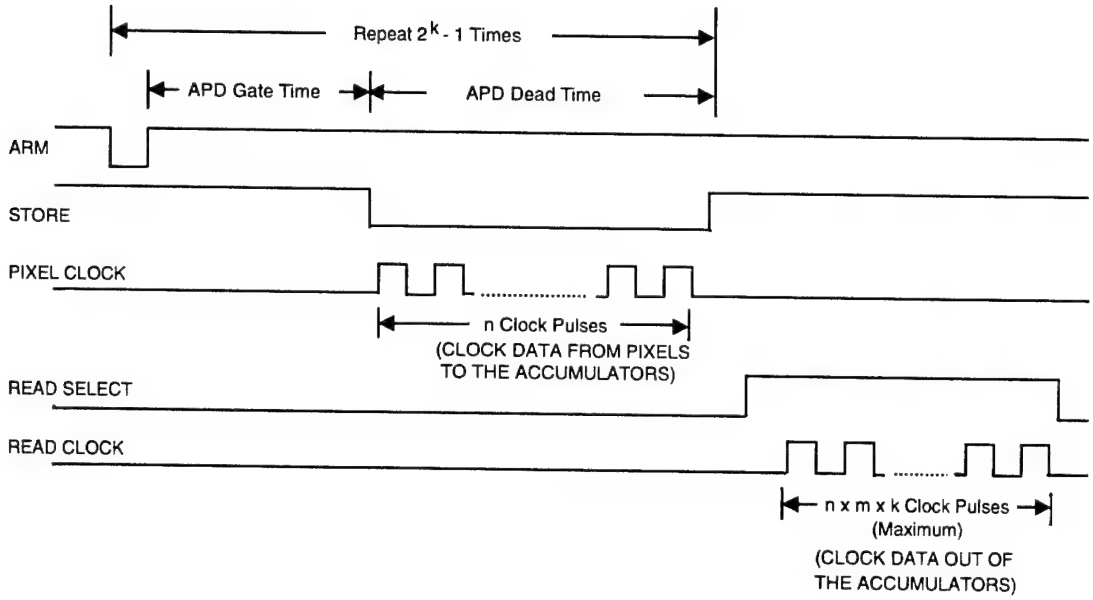

Figure 5-3. Control signal and clocking waveforms for n (row) × m (column) intensity imager shown in Figure 5-2 with k Bit accumulators.

blocks, by adding multiple parallel bitlines and sensing circuitry per pixel column. The size of each block is determined by the desired pixel revisit rate. The multiple blocks of rows could then be read out simultaneously by a larger number of decoders driven by a single binary counter. The scaling is then limited mainly by clock skew, bitline wiring density, and increased power dissipation.

The APD is actively quenched by the positive feedback circuit formed by *p*-channel transistor M5 and *n*-channel transistor M2. The APD from a circuit standpoint behaves as a capacitor and a resistor in parallel. When a photon hits the detector and an avalanche is initiated the charge stored on the capacitor begins to flow through the resistor (actually the APD junction) in parallel with it, and the voltage across the capacitor begins to drop as a result. The *p*-channel transistor M5 senses that drop in voltage across the capacitor, and when the voltage has dropped ~0.5 V, which corresponds roughly to the threshold voltage of M5, the transistor is turned on and begins to charge up the gate of transistor M2. When a sufficient voltage builds up on the gate of M2 the transistor begins to conduct, and now part of the charge stored on the capacitor that represents the APD will flow to ground not via the resistor in parallel with the capacitor but rather through the *n*-channel transistor which has been made to conduct. By using M5 to sense the onset of an avalanche in the APD quickly enough, it is possible to turn on M2, and divert the charge stored on the APD capacitance from flowing through the APD junction and instead to flow via transistor M2 to ground. This action decreases the time required for the carriers to be swept out and limits recombination in the APD junction, since less of the shared charge goes through the junction, but is otherwise diverted via M2 to ground.

When the store-disarm signal (called STORE below) makes a high-to-low transition, the bit value representing whether the APD avalanched or not while it was gated on is stored on the gate of M9 at the same time *p*-channel transistor M7 is turned on, which subsequently turns on *n*-channel transistor M2, which disarms the APD if M2 was not turned on already by an avalanche that was sensed by M5. The disarming of the APD means that its cathode voltage is brought below the breakdown voltage of the device, marking the beginning of the APD dead time or quench time. Regardless of whether the APD avalanched or not while it was armed, the STORE signal stores that value on the gate of M9 and subsequently disarms the APD marking the same start point for the dead time for all APDs in the array, since STORE is globally distributed to all APDs. When STORE is brought high again, the ARM signal can be pulsed low, initiating the process all over again. The APD dead time for all pixels is therefore at least the time interval between the high-to-low transition of STORE and the ARM pulse that rearms the APD.

The timing diagram in Figure 5-3 is specific for a test chip that has been designed. It is worth noting that the disarming of all pixels prior to readout of the entire array is primarily to allow very deterministic conditions to be set for the APDs, and to allow accurate measurements on the array. In future systems, it is anticipated that this practice may not be repeated, therefore allowing much higher duty cycle of the APDs in their armed state, and a higher effective detectivity of the array.

The accumulator has two modes of operation. When data are to be read off the chip, it operates as a shift register that is daisy chained with the other accumulators in a column to transfer the photon-count data out of the accumulator array when clocked by the READ CLOCK input signal. The accumulator accepts a decoder input as well, which is active when pixel data are read from the imaging array to the accumulator array. The accumulator can be any type of flip-flop-based counter k bits in length and able to count to 2^k–1 photons. Considerations of silicon chip area, power dissipation, APD reset time, signal processing overhead, and ultimately the imaging application would dictate the number of bits in the counter and therefore the dynamic range.

By physically placing the accumulator for the pixel outside the pixel area, the pixel size is kept small, thereby improving the resolution of the focal plane array. Controlling the APD gate and quench times in the array allows for an adjustable dead time between reading out all the data from the pixel array to the accumulator array. The dead time of an APD is variable with times as short as 100 ns for high-performance devices and occurs after each triggering or reset of an APD. During the dead time, the APD is blind to photons. The controlled clocking enables the APD dead time to be matched to the readout time. Controlling the APD reset time locally within the pixel will increase the pixel circuit complexity and size. Typically, after 2^k–1 frames have been passed from the pixel array to the accumulators, the digital data in the accumulators are read off chip for further data processing and/or visual display by a computer or other system.

We are submitting prototype designs for manufacture in 0.35-μm CMOS technology with future plans for scaling the designs down to high-speed, low-voltage 0.18-μm and even shorter gate length CMOS processes that would allow manufacture of very high frame rate, large focal plane arrays. The potential applications of photon-counting APD intensity imagers make it important to have a scalable

integrated circuit readout chip architecture that will support different sizes and variations of this intensity imager class.

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6. ANALOG DEVICE TECHNOLOGY

6.1 DELAY-LINE ANALOG-TO-DIGITAL CONVERTER

The demand for higher clock frequencies and dynamic range in fields such as wireless telecommunication requires high-speed and high-accuracy data converters. High-speed analog-to-digital converters (ADCs) have historically been implemented using a flash architecture. However, the number of comparator cells required in a flash ADC grows exponentially with the number of bits. High resolutions (>8 bits) would entail high power consumption, large chip areas, and a large input capacitance, thus restricting flash converters to lower-resolution applications [1].

A survey of ADCs, both commercial and experimental, and the factors limiting performance has been conducted [2]. This survey considers three mechanisms other than quantization noise that limit the achievable signal-to-noise ratio (SNR): input referred thermal noise, comparator ambiguity, and aperture jitter. For ADCs with sampling frequencies between 2 mega-samples per second (MSPS) and 4 giga-samples per second (GSPS), which represents current high-speed, high-resolution converters, the resolution achieved is limited by aperture jitter.

Figure 6-1 shows a novel architecture for high-speed A/D conversion. This block diagram is a variation on the well-known sub-ranging ADC architecture. The first stage consists of a delay line, a subtractor, and an estimation block, which is itself composed of a coarse M-bit ADC, a digital register, and a high-accuracy DAC. The second stage consists of a low-pass reconstruction filter and a sample-and-hold (S/H) circuit followed by a fine N-bit ADC. The ADC outputs from the first and second stage are combined to yield $M+N-1$ total bits of resolution (allowing for one bit of error correction overlap between the two stages). The key difference between the sub-ranging ADC and this new architecture is the addition of the delay line, register, and reconstruction filter. Each of these additions is aimed at reducing the error

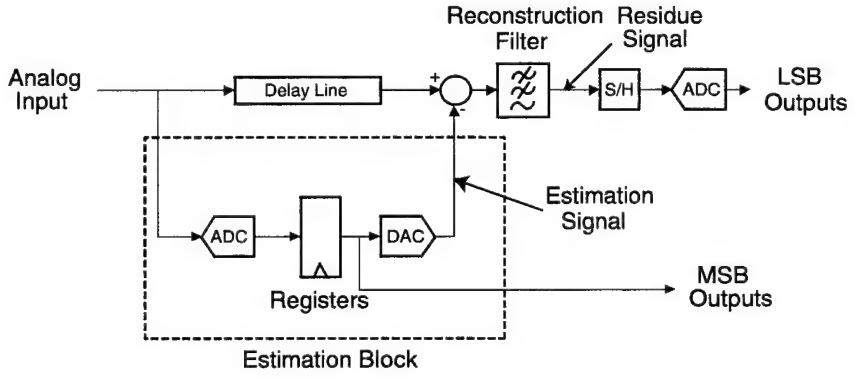

Figure 6-1. Block diagram of delay-line analog-to-digital converter (ADC).

introduced by aperture jitter in the S/H block. Also, the delay-line architecture shares an advantage with the sub-ranging architecture. Since an estimation signal is subtracted from the input, the swing of the residue signal is much smaller than the input. This swing reduction reduces the resolution required of the second-stage ADC and S/H.

The delay is added to eliminate the need for a S/H in the first stage. In a sub-ranging ADC, the input signal can be changing while the estimation block is generating the estimation waveform. Therefore, a S/H is needed at the input to the ADC so that a corresponding input signal and estimation signal are presented to the subtractor. In the delay-line ADC, the delay line is designed to match the delay through the entire estimation block, which is well defined by the clocks. The delayed input signal arrives at the subtractor at the same time as the corresponding estimation signal, eliminating the need for a S/H in the first stage. The other architectural variation, the reconstruction filter, is included to reduce the slope of the input to the second-stage S/H circuit. The input to the S/H in a sub-ranging ADC is the difference between the analog input signal and a coarse, step-like estimate of this signal. This estimate signal contains both the frequencies of interest and also higher harmonic frequencies. The function of the reconstruction filter is to remove these harmonics. In the time domain, the result of the filtering is a smoothing of the residue signal. This smoother signal corresponds to a smaller rate of change, reducing the aperture jitter constraints placed on the second-stage S/H.

Owing to the smoothing function of the reconstruction filter, both the DAC and the reconstruction filter need to be calibrated. To calibrate these two components, the step response of each current source in the DAC is measured after propagating through the reconstruction filter. The measurements are taken over a number of sampling periods until the filter output has settled to the desired accuracy. Given this calibration data, the estimate signal at the output of the filter can be reconstructed by convolving the step responses of a history of DAC input codes. One significant advantage of the calibration process is the elimination of the need for a high-accuracy estimation DAC. Without calibration, the estimation DAC would need to be accurate to $M+N-1$ bits. However, the calibration process measures the inaccuracies of the DAC as well as the filter characteristics. Thus, only an M-bit DAC is required in the estimation block. Another advantage of DAC calibration is glitch correction. Deterministic glitches, caused by timing skew between DAC current sources, are measured by the calibration process and accounted for during signal reconstruction.

The most significant drawback of calibration is the processing required. If the filter step response settles slowly, many samples must be measured and stored, and reconstructing the estimate signal will require the convolution of many known filter step responses. This reconstruction is computationally intensive and is much simpler for a quickly settling filter. However, a filter which settles quickly will not have a very sharp frequency response roll-off. Thus, there is a balance between the complexity of the calibration process and the attenuation of the high-frequency harmonics in the estimate signal. MATLAB simulations have shown that an optimal choice is a 4th-order Butterworth reconstruction filter with a cutoff frequency at 0.6× the sampling frequency of the second-stage ADC. This reconstruction filter allows for a 4-bit estimate signal with a corresponding 4-bit reduction in the maximum signal rate of change while requiring about 8 sampling periods of the second stage in order for the step response to settle to 12-bit accuracy. Note that the estimation block oversamples compared to the sampling frequency of the second

stage, which is the rate at which the delay-line ADC converts data. For the remainder of this report, the sampling rate referred to will be the second-stage data conversion rate.

As mentioned earlier, the main advantage of this ADC architecture is the reduced jitter requirements for the S/H circuit. The requirements on the S/H are relaxed for the reasons mentioned earlier. However, the jitter requirements in the estimation DAC are very strict. Any jitter in clocking the DAC will cause the output of the DAC to be skewed in time from one sample to the next. This error will propagate through the filter and then be converted by the second stage. In effect, the burden of low-jitter clocking is transferred from the S/H circuit in the second stage to the DAC in the first stage. However, unlike S/H clock noise, the effect of clock noise in a DAC may be able to be reduced using clever clocking techniques. Current-steering waveforms, such as those proposed in [3], may be shaped as approximately Gaussian waveforms. Such a Gaussian train is shown in Figure 6-2. The DAC input is clocked when the derivative of the waveform is at its minima. When the DAC input is clocked, the digital code will control which current sources are connected to the output, and the output waveform will have a Gaussian shape of varying amplitudes. This signal will be passed to the reconstruction filter and, after filtering, should be nearly identical to the nonshaped estimate. The clocking technique described will reduce the effect of jitter because the clock transitions occur at instants when the current waveform is changing slowly, so significant aperture jitter will not induce significant error at the DAC output.

An ideal 500-MSPS delay-line ADC has been simulated using MATLAB. The ADCs and DAC were simulated as ideal quantizers. The delay line was a uniform delay and the clocks did not model any jitter. The simulated ADC had a 4-bit estimation stage and an 8-bit second stage. The estimation stage

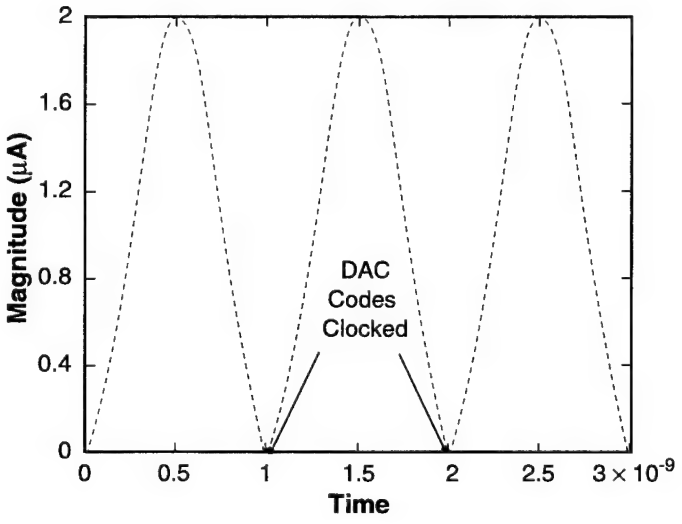

Figure 6-2. Shaped current pulses used in digital-to-analog converter (DAC) to reduce effects of clock jitter.

oversampled by a factor of 2, so it ran at 1 GSPS while data was converted at a 500-MSPS rate. After calibration, the converter achieved approximately 11 effective bits. However, the simulation step size could not be made small enough in order to simulate aperture jitter while still running to completion in a reasonable length of time.

A physical implementation of the delay ADC is currently being built and tested using off-the-shelf components. Prototype specifications have been determined by the availability of commercial high-speed ADCs and DACs. The prototype should be accurate to 11 bits (4-bit estimation and 8-bit second stage). The estimation block runs at 500 MSPS and oversamples by a factor of 2 compared to the second stage, which runs at 250 MSPS. Since a commercial DAC is being used, the use of shaped current pulses to reduce jitter effects is not possible.

Further developments in the delay-line ADC will be needed in order to realize its full potential. One major development would be the integration of the estimation block onto a single chip. Both the estimation ADC and DAC need to be high speed, but they do not need to have very high resolution. Integrated on chip, a simple but high-speed (1–2 GSPS) estimation block could be designed. An integrated solution would also be more power efficient owing to the low accuracy required. Finally, an integrated estimation block would allow the implementation of shaped current pulses in the DAC.

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7. ADVANCED SILICON TECHNOLOGY

7.1 CHARACTERIZATION OF FULLY DEPLETED SOI TRANSISTORS AFTER REMOVAL OF THE SILICON SUBSTRATE

A three-dimensional (3D) integrated circuit technology has been developed that utilizes silicon-on-insulator (SOI) wafers to achieve stacking of multiple circuit layers and unrestricted placement of dense 3D vias [1]. Future 3D integrated circuits will incorporate a fully depleted SOI (FDSOI) CMOS technology to obtain reduced circuit delays and power consumption. The silicon substrate of a fully depleted transistor is an electrode and it is removed during the 3D assembly process. The purpose of this study is to determine the properties of fully depleted transistors from which the silicon substrate has been removed.

FDSOI circuits and test transistors with three levels of metal and transistors were fabricated on an IBIS Advantox190™ wafer. The active (front) side of the wafer was bonded with an adhesive to an oxidized silicon wafer after wafer fabrication and transistor characterization; then the silicon substrate was removed by a silicon wet etch selective to the buried oxide (BOX). The transistors were contacted through pad cuts that were plasma etched through the BOX to expose the back side of metal-1. The optical micrograph of Figure 7-1 is a view through the BOX of a multiplier output circuit and was taken after removing the silicon substrate and etching the pad cuts.

Two-dimensional simulations of FDSOI transistors indicated that removal of the substrate would cause an increase in off-state current. The plot of electric field vectors in Figure 7-2 illustrates that the field from the drain is partially coupled into the substrate. When the substrate is removed those field lines are

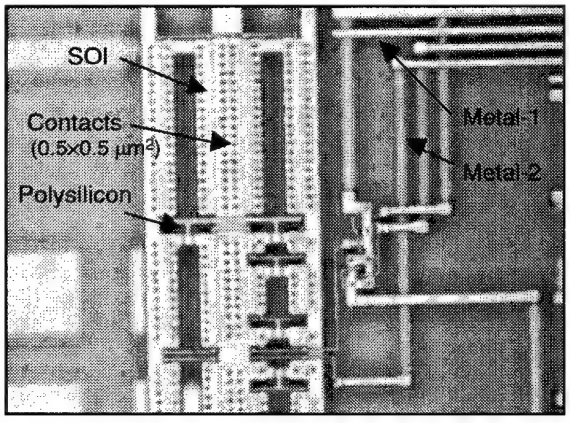

Figure 7-1. Optical micrograph of output circuit viewed through buried oxide (BOX). The metal-1 line is 750 nm wide.

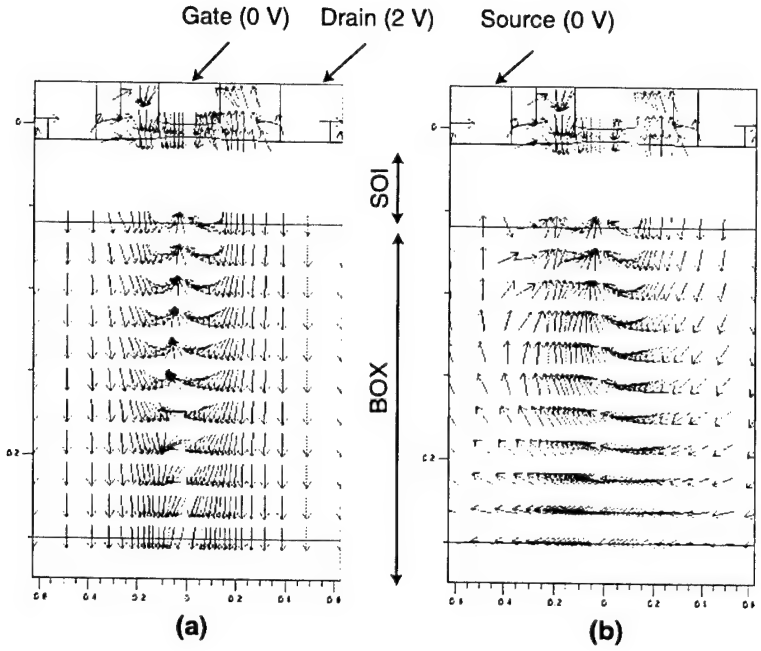

Figure 7-2. Simulated electric field distributions in BOX of 250-nm n-FET (a) with and (b) without substrate. The silicon substrate is at 0 V in (a).

restricted to the BOX causing a reduction in the potential barrier in the channel near the SOI-BOX interface leading to increased source-drain leakage. The measurements in Figure 7-3(a) show the effect of removing the silicon substrate on off-state currents for both *n*- and *p*-channel transistors with drains biased at 2 and –2 V, respectively, and the remaining terminals at 0 V. A comparison of the transfer characteristics of 500-nm transistors shown in Figures 7-3(b) and 7-3(c) indicates that removal of the substrate decreased the threshold of the main channel of the *n*-FET by 50 mV and the *p*-FET by –95 mV and would explain the differences in off-state leakage. The change in thresholds was likely caused by plasma damage that occurred during pad etch. The plasma damage had a greater effect on leakage than removal of the silicon substrate and is normally removed by a 400°C sinter, but the thermal stability of the adhesive bond precluded a sinter.

The wafer was also used to determine whether removal of the substrate would modify the response of FDSOI transistors to ionizing radiation. Edgeless *n*-channel transistors with body contacts were irradiated and the results were compared with data previously obtained from an Advantox190™ wafer processed in the same fabrication run. Radiation testing was conducted using a 10-keV X-ray tube in an Aracor 4100. The transistors were biased in the off-gate condition (drain bias at 2 V, all other terminals grounded). The transistors were tested before irradiation and after incremental X-ray doses of 5, 10, 20, 50,

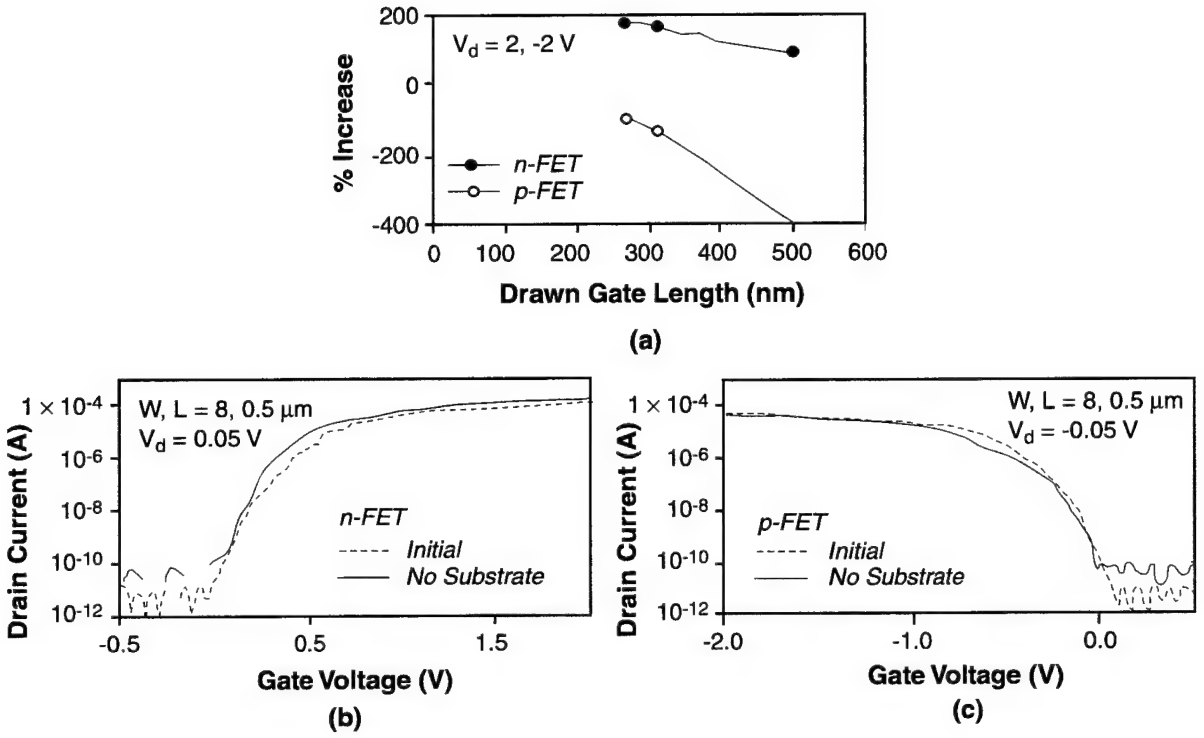

Figure 7-3. Increase in off-state current of mesa-isolated fully depleted silicon-on-insulator (FDSOI) transistors after removal of silicon substrate is shown in (a); a negative value represents a decrease. As indicated in (b) and (c), positive charge created during plasma etching of the BOX is responsible for the change.

100, 200, 500, and 1000 krad (Si). The data shown in Figures 7-4(a) and 7-4(b) indicate a significant reduction in sensitivity to ionizing radiation after removal of the substrate. A comparison of threshold as a function of total dose is shown in Figure 7-4(c). The decrease in threshold after 1000 krad was 600 and 20 mV for the transistors with and without the silicon substrate, respectively. The threshold was defined as the gate voltage required to conduct a drain current of 10^{-7} A with a 50-mV drain bias and a gate width-to-length ratio of unity. A previous study indicated that hole trapping in the BOX that decreased the back-channel threshold of *n*-channel FDSOI transistors was the principal factor affecting the response of FDSOI transistors to ionizing radiation [2]. The field distribution shown in Figure 7-2(a) suggests that electrons generated in the BOX during irradiation would drift towards the SOI film where they could escape, and a fraction of the holes would drift towards the SOI-BOX interface in the channel region and decrease the back-channel threshold. In Figure 7-2(b) we see that removal of the substrate would create a field pattern that confines the electrons and holes within the BOX, and leads to greater recombination of the charge generated by radiation.

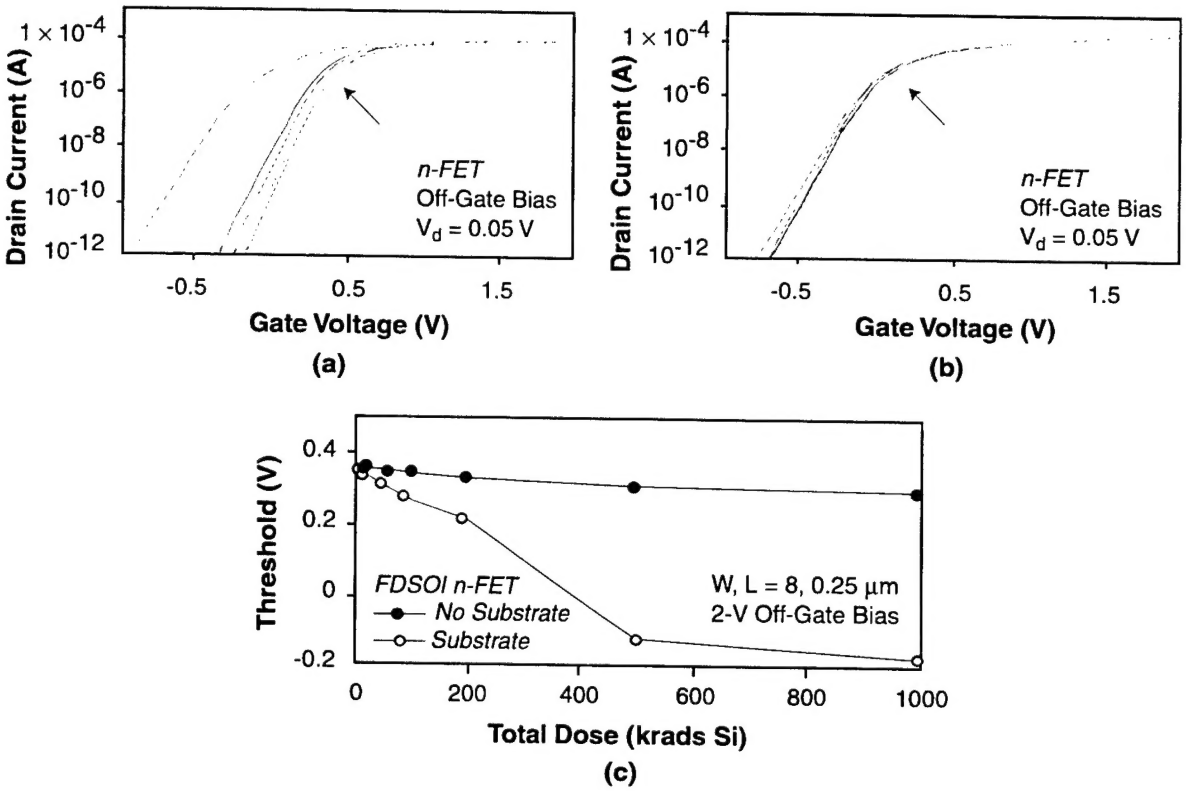

Fig. 7-4. Total dose effects on H-gate transistors with 250-nm gate lengths and body contacts (a) with and (b) without substrate; the arrows indicate the direction of increasing total dose up to 1 Mrad (Si). In (c) the same total dose sequence was used to determine threshold variation as a function of total dose.

Scattering (S) parameters were measured before and after substrate removal to determine the effect of the substrate on the rf properties of FDSOI transistors. They were measured by on-wafer probing and a network analyzer up to 50 GHz. The ground-signal-ground rf probing pads measure 50 × 60 μm each and are separated by 50 μm. The input reflection S parameters (S_{11}) of the probing pads were measured before and after wafer thinning. The probe pads were modeled as a series RC network with the probe pads capacitively coupled to the conductive substrate. The initial pad capacitance was 14.5 fF. After removing the silicon substrate and bonding to a quartz wafer, the pad capacitance was reduce to 2.5 fF with an infinite series resistance.

Intrinsic device characteristics were obtained by de-embedding the pad capacitance from measured S parameters and were called the as-measured data. The as-measured and de-embedded S_{11} of an *n*-MOSFET before thinning differed significantly. After substrate removal, the as-measured S_{11} data for the MOSFET were nearly identical to the de-embedded data before thinning, confirming negligible

TABLE 7-1
Measured f_T and f_{max} (GHz) of *n*- and *p*-MOSFETs

Si Substrate	Data (GHz)	*n*-MOSFET 2×5 μm	*n*-MOSFET 10×20 μm	*p*-MOSFET 2×5 μm
Present	f_T, as measured	27.9	35.6	19.5
	f_T, de-embedded	60.7	38.7	38.6
Removed	f_T, as measured	61.4	36	40
	f_T, de-embedded	61.4	36	40
Present	f_{max}, as measured	16.7	7.9	15.5
	f_{max}, de-embedded	34.3	8.5	26.1
Removed	f_{max}, as measured	33.4	8.2	23.2
	f_{max}, de-embedded	33.4	8.2	23.2

capacitance from the pad to the quartz substrate. Closely matched results of cut-off frequency (f_T) and the maximum frequency of oscillation (f_{max}) for MOSFETs with and without the Si substrate are listed in Table 7-1.

Any anticipated improvement in rf performance of the MOSFET, under the presumption that the source/drain junction capacitance was reduced after removing the Si substrate, was not observed in the experiment. One plausible explanation is that the junction capacitance of a FDSOI MOSFET, dominated by the BOX capacitor, is insignificantly small even on a conductive Si substrate. This unique feature favors FDSOI for high-speed analog and rf applications. In addition, removing the Si substrate substantially reduced the parasitic capacitance associated with the interconnect metallization.

FDSOI technology is compatible with the construction of 3D integrated circuits. Removal of the silicon substrate, an essential step in the 3D assembly technology, will not cause an increase in off-state current provided the wafer bond technology is compatible with a 400°C sinter. Substrate removal will also decrease the effect of ionizing radiation on transistor properties as well as improve rf performance.

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This report covers in detail the research work of the Solid State Division at Lincoln Laboratory for the period 1 August–31 October 2001. The topics covered are Quantum Electronics, Electro-optical Materials and Devices, Submicrometer Technology, Biosensor and Molecular Technologies, Advanced Imaging Technology, Analog Device Technology, and Advanced Silicon Technology. Funding is provided by several DoD organizations—including the Air Force, Army, MDA, DARPA, Navy, NSA, and OSD—and also by the DOE, NASA, and NIST.

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